DDR 13-Bit to 26-Bit Registered Buffer

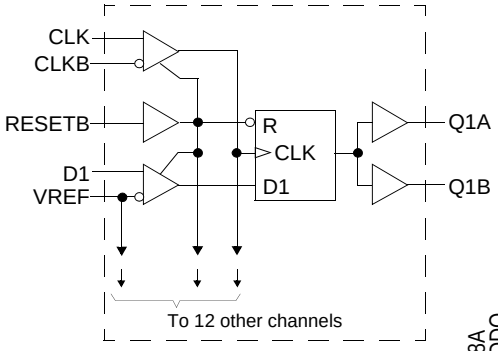
Features

- Differential clock signals
- Meets SSTL_2 class II specifications on outputs
- Low voltage operation – V_{DD} = 2.3 V to 2.7 V
- Available in 64-pin TSSOP and 56-pin VFQFN packages (MLF2)

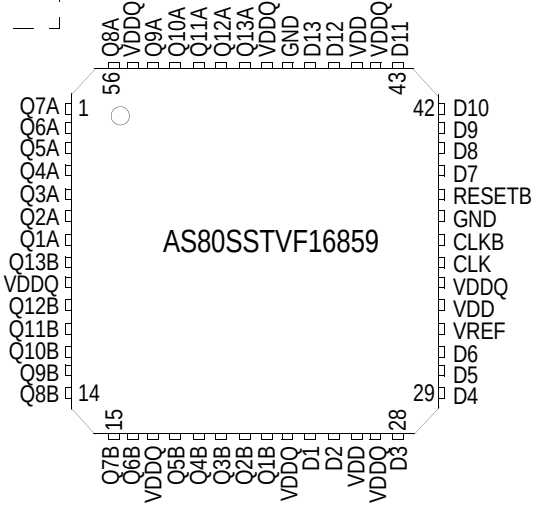
Recommended Applications

- DDR memory modules: PC1600, PC2100, PC2700, AND PC3200
- Provides complete DDR DIMM logic solution with PCV857
- SSTL_2-compatible data registers

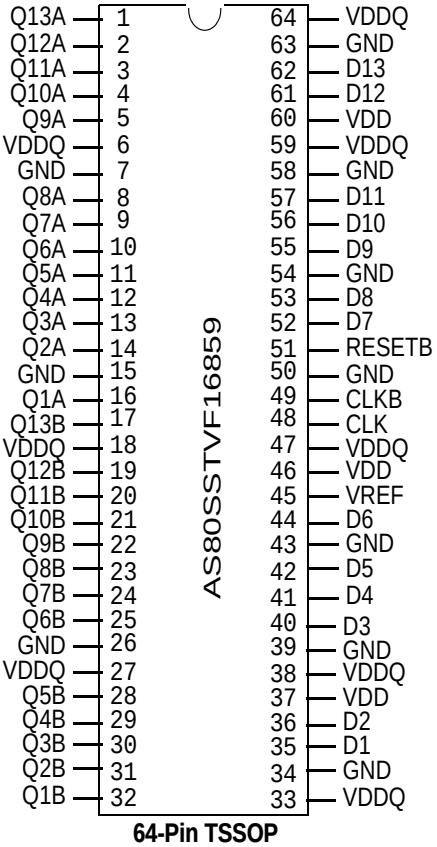
Block Diagram



Pin Configurations



56-Pin VFQFN (MLF2)



64-Pin TSSOP
6.10 mm body, 0.50 mm pitch

Truth Table[1]

Inputs				Q outputs
RESETB	CLK	CLKB	D	Q
L	X or floating	X or floating	X or floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0[2]

1 H = high signal level, L = low signal level, ↑ = transition low to high, ↓ = transition high to low, X = don't care.
2 Output level before the indicated steady state input conditions were established.

Description

The 13-bit to 26-bit PC16859 is a universal bus driver designed for 2.3 V to 2.7 V V_{DD} operation and SSTL_2 I/O levels, except for the LVCMOS RESETB input.

Data flow from D to Q is controlled by the differential clock (CLK/CLKB) and a control signal (RESETB). The positive edge of CLK is used to trigger the data flow, and CLKB is used to maintain sufficient noise margins, whereas RESETB, an LVCMOS asynchronous signal, is intended for use only at power-up. PC16859 supports low-power standby operation. A logic level low at RESETB assures that all internal registers and outputs (Q) are reset to the logic low state, and that all input receivers, data (D), and clock (CLK/CLKB) are switched off. Note that RESETB must always be supported with LVCMOS levels at a valid logic state because VREF may not be stable during power-up.

To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESETB must be held at a logic low level during power-up.

In the DDR DIMM application, RESETB is specified to be completely asynchronous with respect to CLK and CLKB, therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby state, the register will be cleared and the outputs will be driven to a logic low level quickly relative to the time to disable the differential input receivers. This ensures there are no glitches on the output. When coming out of low power standby state, however, the register will become active quickly relative to the time to enable the differential input receivers. When the data inputs are at a logic level low and the clock is stable during the low-to-high transition of RESETB until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic low level.

Pin Configuration (64-Pin TSSOP)

Pin number	Pin name	Type	Description
1, 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 16, 17, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31, 32	Q(13:1)	Output	Data output
7, 15, 26, 34, 39, 43, 50, 54, 58, 63	GND	PWR	Ground
6, 18, 27, 33, 38, 47, 59, 64	VDDQ	PWR	Output supply voltage, 2.5 V nominal
35, 36, 40, 41, 42, 44, 52, 53, 55, 56, 57, 61, 62	D(13:1)	Input	Data input
48	CLK	Input	Positive master clock input
49	CLKB	Input	Negative master clock input
37, 46, 60	VDD	PWR	Core supply voltage, 2.5 V nominal
51	RESETB	Input	Reset (active low)
45	VREF	Input	Input reference voltage, 1.25 V nominal

Pin Configuration (56-Pin MLF2)

Pin number	Pin name	Type	Description
1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 50, 51, 52, 53, 54, 56	Q(13:1)	Output	Data output
37, 48	GND	PWR	Ground
9, 17, 23, 27, 34, 44, 49, 55	VDDQ	PWR	Output supply voltage, 2.5 V nominal
24, 25, 28, 29, 30, 31, 39, 40, 41, 42, 43, 46, 47	D(13:1)	Input	Data input
35	CLK	Input	Positive master clock input
36	CLKB	Input	Negative master clock input
26, 33, 45	VDD	PWR	Core supply voltage, 2.5 V nominal
38	RESETB	Input	Reset (active low)
32	VREF	Input	Input reference voltage, 1.25 V nominal
–	Center pad	PWR	Ground (VFQFN package only)

Absolute Maximum Ratings

Storage temperature	- 65° C to +150° C
Supply voltage	-0.5 to 3.6 V
Input voltage[1]	-0.5 to V_{DD} + 0.5
Output voltage[1,2]	-0.5 to V_{DD} + 0.5
Input clamp current	± 50 mA
Output clamp current	± 50 mA
Continuous output current	± 50 mA
V_{DD}, V_{DDQ}, or GND current/pin	± 100 mA
Package thermal impedance[3]	55° C/W

1 The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2 This current will flow only when the output is in the high state level $V_0 > V_{DDQ}$.
3 The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only, and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions - DDRI / DDR333 (PC1600, PC2100, PC2700)

Guaranteed by design. Not 100% tested in production.

Parameter	Description		Min	Typ	Max	Units
V_{DD}	Supply voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O supply voltage		2.3	2.5	2.7	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input voltage		0		V_{DD}	V
$V_{IH(DC)}$	DC input high voltage	Data inputs	V_{REF} + 0.15			V
$V_{IH(AC)}$	AC input high voltage		V_{REF} + 0.31			V
$V_{IL(DC)}$	DC input low voltage				V_{REF} - 0.15	V
$V_{IL(AC)}$	AC input low voltage				V_{REF} - 0.31	V
V_{IH}	Input high voltage level	RESETB	1.7			V
V_{IL}	Input low voltage level				0.7	V
V_{ICR}	Common mode input range	CLK. CLKB	0.97		1.53	V
V_{ID}	Differential input voltage		0.36			V
V_{IX}	Cross-point voltage of differential clock pair		(V_{DDQ}/2) - 0.2		(V_{DDQ}/2) + 0.2	V
I_{OH}	High-level output current				-20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	° C

Recommended Operation Conditions - DDRI-400 (PC3200)

Guarenteed by design, not 100% tested in production.

Parameter	Description		Min	Typ	Max	Units
V_{DD}	Supply Voltage		2.5	2.6	2.7	V
V_{DDQ}	I/O supply voltage		2.5	2.6	2.7	V
V_{REF}	Reference voltage		1.25	1.3	1.35	V
V_{TT}	Termination voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input voltage		0		V_{DDQ}	V
$V_{IH(DC)}$	DC input high voltage	Data Inputs	V_{REF} + 0.15			V
$V_{IH(AC)}$	AC input high voltage		V_{REF} + 0.31			V
$V_{IL(DC)}$	DC input low voltage				V_{REF} - 0.15	V
$V_{IL(AC)}$	AC input low voltage				V_{REF} - 0.31	V
V_{IH}	Input high voltage level	RESETB	1.7			V
V_{IL}	Input low voltage level				0.7	V
V_{ICR}	Common mode input range	CLK, CLKB	0.97		1.53	V
V_{ID}	Differential input voltage		0.36			V
V_{IX}	Cross-point voltage of differential clock pair		(V_{DDQ}/2) - 0.2		(V_{DDQ}/2) + 0.2	V
I_{OH}	High-level output current				-16	mA
I_{OL}	Low-level output current				16	mA
T_A	Operating free-air temperature		0		70	° C

DC Electrical Characteristics - DDRI / DDR333 (PC1600, PC2100, PC2700)

TA = 0° C to 70° C, V_{DD} = 2.5 ± 0.2 V, and V_{DDQ} = 2.5 ± 0.2 V (unless otherwise stated)

Guaranteed by design. Not 100% tested in production..

Symbol	Parameters	Test conditions		VDD	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.3 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.3 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -16 mA		2.3 V	1.95			V
V_{OL}		I_{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.3 V			0.35	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.7 V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle		2.7 V		30		µA/ clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle One data input switching at half clock frequency, 50% duty cycle		2.7 V		10		µA/ clock MHz/ data input
r_{OH}	Output high	I_{OH} = -20 mA		2.3 V to 2.7 V	7		20	Ω
r_{OL}	Output low	I_{OL} = 20 mA		2.3 V to 2.7 V	7		20	Ω
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.5 V			4	Ω
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV, V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV		2.5 V	2.5		3.5	pF
	CLK and CLKB			2.5 V	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.5V	2.5		3.5	pF

DC Electrical Characteristics - DDRI-400 (PC3200)

TA = 0° C to 70° C, V_{DD} = 2.6 ± 0.1 V, and V_{DDQ} = 2.6 ± 0.1 V (unless otherwise stated)

Guaranteed by design. Not 100% tested in production..

Symbol	Parameters	Test conditions		VDD	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.5 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.5 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -8 mA		2.5 V	1.95			V
V_{OL}		I_{OL} = 100 µA		2.5 V to 2.7 V			0.2	V
		I_{OL} = 8 mA		2.5 V			0.35	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.7 V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle		2.7 V		30		µA/ clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle One data input switching at half clock frequency, 50% duty cycle		2.7 V		10		µA/ clock MHz/ data input
r_{OH}	Output high	I_{OH} = -16 mA		2.5 V to 2.7 V	7		20	Ω
r_{OL}	Output low	I_{OL} = 16 mA		2.5 V to 2.7 V	7		20	Ω
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.6 V			4	Ω
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV, V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV		2.6 V	2.5		3.5	pF
	CLK and CLKB			2.6 V	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.6V	2.5		3.5	pF

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted.)

Guaranteed by design. Not 100% tested in production

* This parameter is not necessarily production tested..

Symbol	Parameters		V_{DDQ} = 2.5V±0.2V		V_{DDQ} = 2.6V±0.1V		Units
			Min	Max	Min	Max	
f_{CLOCK}	Clock frequency			200		270	MHz
t_W	Pulse duration, CK, CKLB high or low		2.5		2.5		ns
t_{ACT}*	Differential inputs active time[1]			22		22	ns
t_{INACT}*	Differential inputs inactive time[2]			22		22	ns
t_S	Setup time, fast slew rate[3,5]	Data before CLK↑, CLKB↓	0.75		0.4		ns
	Setup time, slow slew rate[4,5]		0.9		0.6		ns
t_h	Hold time, fast slew rate[3,5]	Data after CLK↑, CLKB↓	0.75		0.4		ns
	Hold time, slow slew rate[4,5]		0.9		0.6		ns

1 Data inputs must be low a minimum time of t_{ACT} max, after RESETB is taken high

2 Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max, after RESETB is taken low

3 For data signal input slew rate ≥ 1 V/ns

4 For data signal input slew rte ≥ 0.5 V/ns and < 1 V/ns

5 CLK, CLKB signals iput slew rates are ≥ 1 V/ns

Switching Characteristics - DDRI / DDR333 (PC1600, PC2100, PC2700)

(Over recommended operating free-air temperature range unless otherwise noted.)

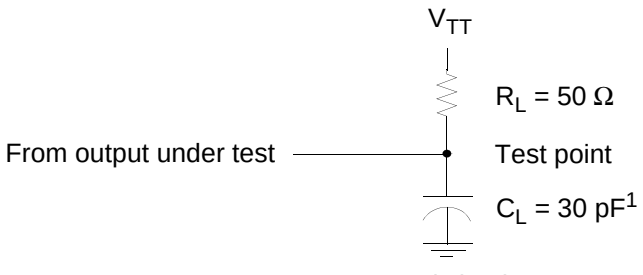
Symbol	From (input)	To (output)	VDD = 2.5 V ± 0.2 V			Units
			Min	Typ	Max	
f_{max}			200	–	–	MHz
t_{PD}	CLK, CLKB (TSSOP)	Q	1.1		2.8	ns
	CLK, CLKB (VFQFN[MLF2])	Q	1.1		2.8	ns
t_{phl}	RESETB	Q	–	–	5.0	ns

Switching Characteristics - DDRI-400 (PC3200)

(Over recommended operating free-air temperature range unless otherwise noted.)

Symbol	From (input)	To (output)	VDD = 2.6 V ± 0.1 V			Units
			Min	Typ	Max	
f_{max}			210			MHz
t_{PD}	CLK, CLKB (VFQFN[MLF2]) Simultaneous switching	Q	1.1		2.2	ns
t_{PDSS}		Q			2.48	ns
t_{phl}	RESETB	Q			3.5	ns

Parameter Measurement Information (V_{DD} = 2.5 V ± 0.2 V)



[1] C_L includes probe and jig capacitance.

Voltage and Current Waveforms

In the following waveforms, note that all input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

The outputs are measured one at a time with one transition per measurement.

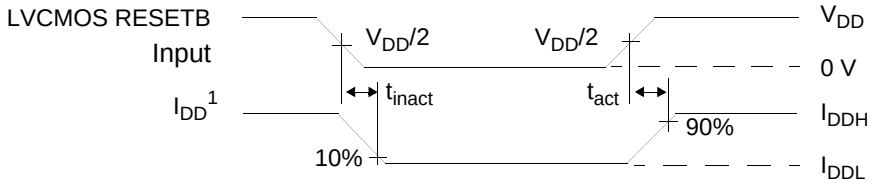
$V_{TT} = V_{REF} = V_{DDQ}/2$.

$V_{IH} = V_{REF}$ + 310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

$V_{IL} = V_{REF}$ - 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

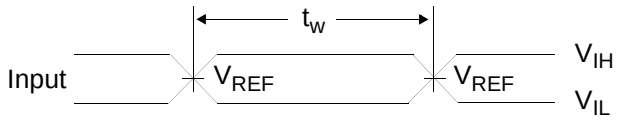
t_{PLH} and t_{PHL} are the same as t_{pd}.

Input active and inactive times

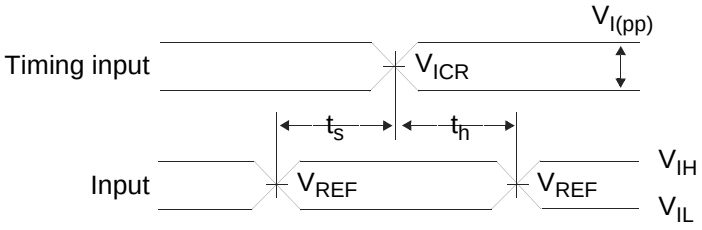


[1] I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

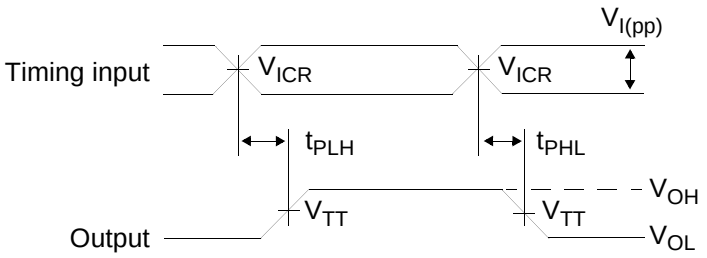
Pulse duration

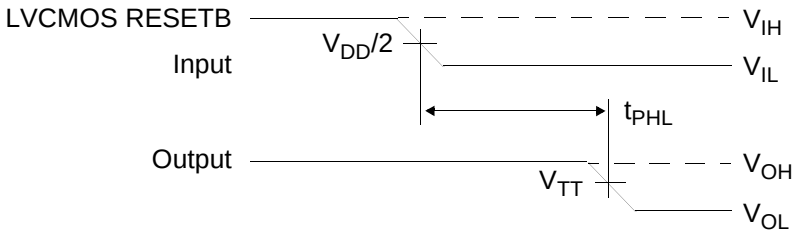


Setup and hold times

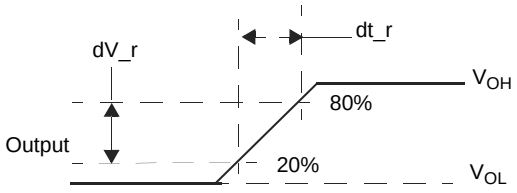


Propagation delay times

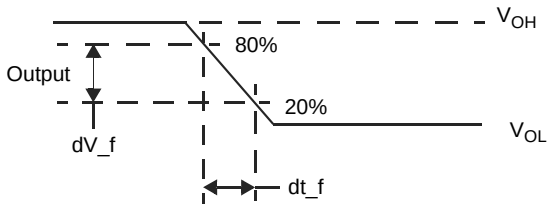




LOW-TO-HIGH SLEW RATE MEASUREMENT



HIGH-TO-LOW SLEW-RATE MEASUREMENT



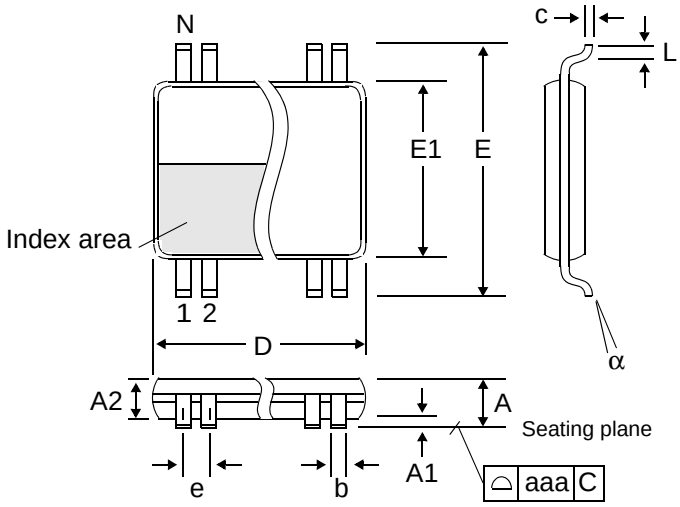
Output slew rates over recommended operating free-air temperature range (unless otherwise noted)

Parameter	From	To	V_{CC}= 2.5 V ± 0.2V *		V_{CC} = 2.6 V ± 0.1 V *		Unit
			Min	Max	Min	Max	
dV/dt_r	20%	80%	1	4	1	4	V/ns
dV/dt_f	80%	20%	1	4	1	4	V/ns
dV/dt_Δ**	20% or 80%	80% or 20%		1		1	V/ns

*For this test condition, V_{DDQ} is always equal to V_{DD}

**Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

Package Dimensions (64- Pin TSSOP)



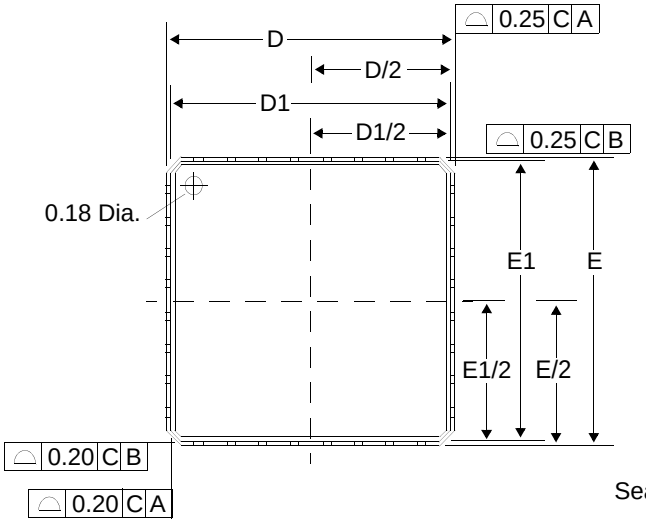
6.10 mm (240 mil) body,
0.50 mm (0.020 mil) pitch TSSOP

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.32	0.041
b	0.17	0.27	0,007	0.011
c	0.09	0.20	0.0035	0.008
D	See variations below			
E	8.10 basic		0.319 basic	
E1	6.00	6.20	0.236	0.244
e	0.50 basic		0.020 basic	
L	0.45	0.75	0.018	0.030
N	See variations below			
α	0°	8°	0°	8°
aaa	–	0.10	–	0.004

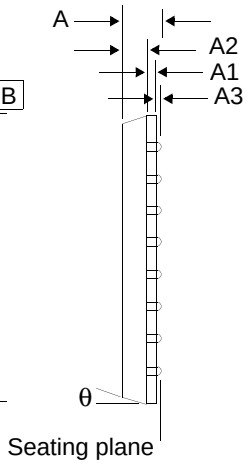
Variations:

N	D (mm)		D (inch)	
	Min	Max	Min	Max
64	16.90	17.10	0.665	0.673

Package Dimensions (56-Pin MLF2)

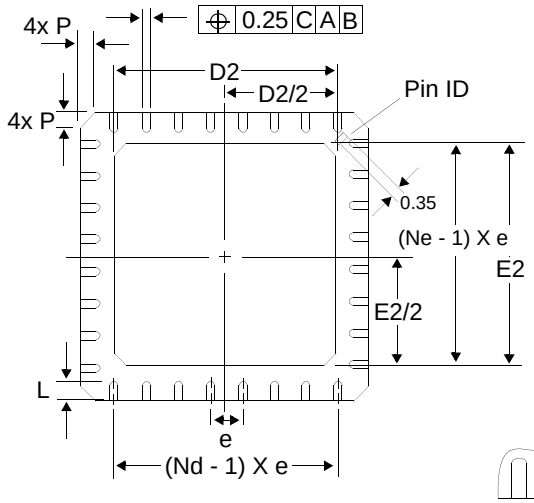


Top view

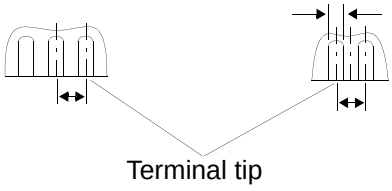


Side view

Symbol	Common dimensions		
	Min	Typ	Max
A		0.85	1.00
A1	0.00	0.01	0.05
A2		0.65	0.80
A3	0.20 BSC		
D	8.00 BSC		
D1	7.75 BSC		
E	8.00 BSC		
E1	7.75 BSC		
θ			12
P	0.24	0.42	0.60
R	0.13	0.17	0.23
Pitch variation D			
e	0.50 BSC		
N	56		
Nd	14		
Ne	14		
L	0.30	0.40	0.50
b	0.18	0.23	0.30
Q	0.00	0.20	0.45
D2	4.35	4.50	4.65
E2	5.05	5.20	5.35

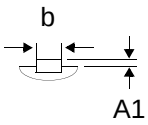


Bottom view



Terminal tip

For odd terminal/side For even terminal/side



Cross section

Ordering Information

Ordering Number	Marking	Package	Qty per Reel	Temperature
AS80SSTVF16859-64TT	AS80SSTVF16859T	64-Pin TSSOP, Tube		0°C to 70°C
AS80SSTVF16859-64TR	AS80SSTVF16859T	64-Pin TSSOP, Tape & Reel	2500	0°C to 70°C
AS80SSTVF16859-56KT	AS80SSTVF16859K	56-pin MLF2, Tube		0°C to 70°C
AS80SSTVF16859-56KR	AS80SSTVF16859K	56-pin MLF2, Tape & Reel	2500	0°C to 70°C